High-Mobility Holes in Dual-Gated WSe_2 Field-Effect Transistors

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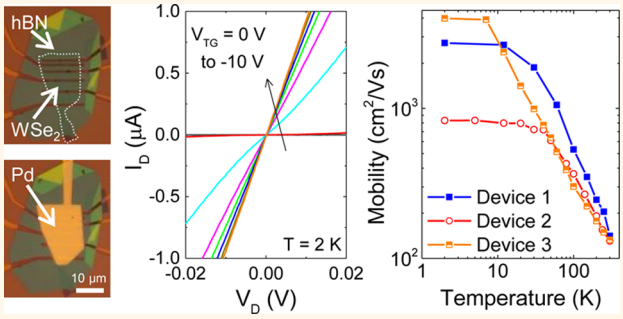
ABSTRACT We demonstrate dual-gated p-type field-effect transistors (FETs) based on few-layer tungsten diselenide (WSe_2) using high work-function platinum source/drain contacts and a hexagonal boron nitride top-gate dielectric. A device topology with contacts underneath the WSe_2 results in p-FETs with I_{ON}/I_{OFF} ratios exceeding 10^7 and contacts that remain ohmic down to cryogenic temperatures. The output characteristics show current saturation and gate tunable negative differential resistance. The devices show intrinsic hole mobilities around 140 $cm^2/(V\,s)$ at room temperature and approaching 4000 $cm^2/(V\,s)$ at 2 K. Temperature-dependent transport measurements show a metal−insulator transition, with an insulating phase at low densities and a metallic phase at high densities. The mobility shows a strong temperature dependence consistent with phonon scattering, and saturates at low temperatures, possibly limited by Coulomb scattering or defects.



KEYWORDS: transition metal dichalcogenide (TMD) · tungsten diselenide (WSe_2) · field-effect transistor (FET) · metal−insulator transition (MIT) · hole mobility

The isolation of graphene and study of its exceptional properties has triggered an interest in several other two-dimensional (2D) layered materials,[1] semiconducting transition metal dichalcogenides (TMDs)[2,3] being one of them. In contrast to graphene's zero band gap, semiconducting TMDs have a large (1−2 eV) band gap, making them potentially useful for future electronic devices requiring high I_{ON}/I_{OFF} ratios. The diverse variety of semiconducting TMDs such as molybdenum disulfide (MoS_2),[4,5] molybdenum diselenide ($MoSe_2$),[6] tungsten disulfide (WS_2),[7] and tungsten diselenide (WSe_2),[8−11] each having its own thickness-dependent electronic band-structure, provide a wide choice for specific use in optoelectronic, low-power, and/or high-performance device applications.[5,9,12] In addition, the coupled spin and valley degrees of freedom and massive charge carriers in TMDs result in a wealth of novel electrical and optoelectronic phenomena[13,14] that can be exploited for the development of alternative device architectures.[15,16] To date, MoS_2 has received the most attention among all TMD field-effect transistors (FETs), with the devices exhibiting n-type conduction.[4,5,17−20] It is equally important to explore p-type TMDs, in order to realize a practical TMD-based post-silicon CMOS architecture. One TMD that has attracted significant attention for p-FETs is WSe_2, with early reports of bulk-WSe_2 FETs showing hole mobilities approaching 500 $cm^2/(V\,s)$.[11] Subsequently, few-layered WSe_2 FETs have also been demonstrated with high I_{ON}/I_{OFF} ratios and hole mobilities.[8,10,21−23] While $MoTe_2$[24] and 2D black phosphorus[25] have also been reported to show p-type conduction, these materials are less stable in ambient conditions. The high thermal and environmental stability and well-developed materials science of WSe_2 make it very attractive as a channel material for 2D p-FETs.[11]

Creating low-resistance, ohmic contacts has been a major challenge limiting study of the intrinsic properties of TMDs. Most metal contacts to TMDs form Schottky barriers, resulting in large series resistances, which degrade even further at low temperatures.[5,9,10] Considerable research effort has been put into addressing this problem, using techniques such as metal work-function tuning,[5,9,26] contact annealing,[17,18] graphene contacts,[21,27,28]

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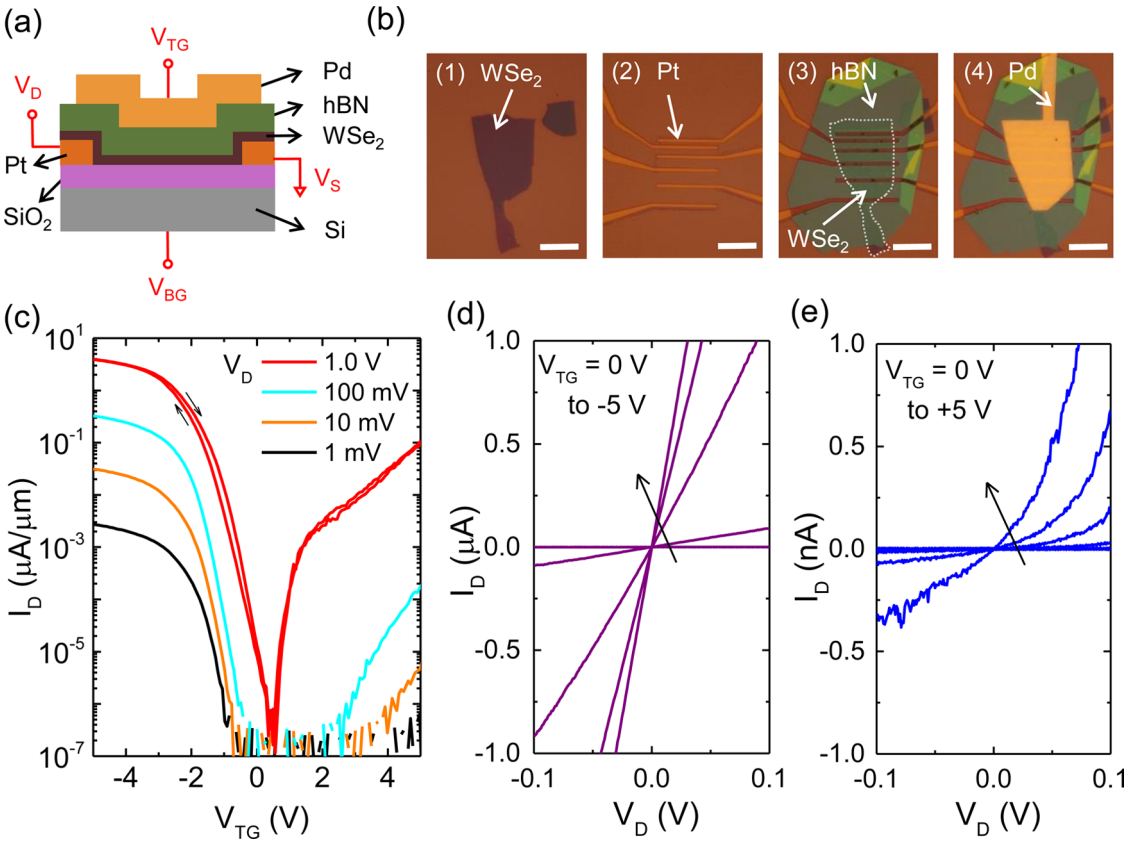

Figure 1. (a) Schematic of a dual-gated WSe_2 FET with Pt contacts underneath the WSe_2, an hBN top-gate dielectric, and a Pd top-gate. The biasing scheme is shown in red. (b) Optical micrographs during the fabrication process show (1) a three/four-layer exfoliated WSe_2 flake on SiO_2/Si and (2) prepatterned Pt contacts on a separate SiO_2/Si substrate. (3) An hBN flake is used to pick up the WSe_2 and is transferred onto the Pt contacts, followed by (4) patterning of a local Pd top gate. The scale bars are 10 μm. (c) Transfer characteristics of the FET (L = 6 μm) at different V_D, showing p-type conduction at V_D as low as 1 mV and an I_{ON}/I_{OFF} ratio > 10^7 at V_D = 1 V. Low-bias output characteristics of the FET at different V_{TG} for the (d) p-branch and (e) n-branch show ohmic and Schottky contacts, respectively. The back-gate is grounded for all measurements.

electrical double layer (EDL) structures,[21,23,28] and doped source/drain contacts.[8] While improving the contacts, these techniques however have several limitations such as (i) processing constraints and instability of low work-function metals,[5,9] (ii) unintentional doping during contact annealing,[18] (iii) slow response speed of EDL structures, preventing their use in FETs,[23] and (iv) instability of surface charge transfer dopants in air.[8] Whereas graphene contacts result in efficient electron injection in MoS_2,[27] the large band offsets between the Dirac point of graphene and the conduction and valence bands of WSe_2[29] necessitate additional doping of the graphene for efficient carrier injection.[21,28] Moreover, these approaches are primarily directed toward back-gated FET geometries, which are of limited use in practical circuits. There is a need to develop top-gated FET structures in order to enable independent control of multiple FETs on the same substrate toward large-scale device integration. Furthermore, an air-stable, low-temperature-compatible contact scheme is imperative for a systematic investigation of the nature of charge transport in WSe_2.

In this work, we use high work-function platinum (Pt) as the contact metal for efficient hole injection into the valence band of WSe_2. By using a device topology with the Pt contacts underneath the WSe_2, and a pristine hexagonal boron nitride (hBN) top-gate dielectric, we realize dual-gated FETs with contacts that are ohmic down to cryogenic temperatures. We demonstrate that this contact scheme is optimized for top-gated FET operation, with the back-gate serving as an additional knob to fine-tune the FET characteristics. Top-gated transfer characteristics show I_{ON}/I_{OFF} ratios exceeding 10^7 and hole mobilities around 140 $cm^2/(V\,s)$ at room temperature in three/four-layer WSe_2. The output characteristics exhibit current saturation and a negative differential resistance. Temperature-dependent transport measurements reveal a metal–insulator transition, indicating high device quality. The mobility shows a strong temperature dependence at high temperatures, indicative of phonon-dominated transport in this regime. At low temperatures, the mobility saturates, approaching up to 4000 $cm^2/(V\,s)$, possibly limited by Coulomb scattering or defects.[18,21]

RESULTS AND DISCUSSION

We use exfoliated WSe_2 flakes derived from commercially available crystals as the source material for

fabricating the FETs in this work. Three/four-layer WSe_2 and 15−20 nm hBN flakes are identified using optical contrast, Raman spectroscopy, and photoluminescence measurements (S1 in the Supporting Information). A polymer-coated silicone stamp[30] is used to assemble and transfer a stack of hBN/WSe_2 on to prepatterned Cr/Pt electrodes on a SiO_2/Si substrate. Subsequently, a local palladium (Pd) top-gate is patterned, resulting in a device structure as shown in Figure 1a. Optical micrographs during the fabrication process are shown in Figure 1b and described in detail in the Materials and Methods section.

We chose Pt due to its high work-function ($\Phi_M \approx$ 6.0 eV),[31] which places its Fermi level below the valence band edge of WSe_2 ($\chi_{WSe_2} + E_g \approx$ 5.5 eV).[29]This band alignment is intuitively expected to result in ohmic p-type contacts. The choice of appropriate work-function metals has been successfully employed in the past to optimize carrier injection in TMD FETs. Low work-function scandium contacts were found to result in efficient electron injection in MoS_2,[5] and indium was used for low-resistance n-type contacts to WSe_2.[9] However, Fermi level pinning at the metal−TMD interface has also been found to strongly impact the contacts, resulting in nontrivial behavior for some metal−TMD combinations.[5,9] Furthermore, the metal−TMD interface is highly sensitive to the processing environment such as vacuum conditions in the deposition chamber, deposition rate, and metal topography. These variations can potentially affect the TMD electronic structure, metal crystallinity, and, in turn, the metal work-function,[32] resulting in wide variations in FET characteristics among reports in the literature.[5,9,22] By choosing an inert contact metal such as Pt, and by decoupling the metal deposition step from creating the actual metal−TMD contact, we can potentially eliminate some of these uncertainties. Direct deposition of Pt on WSe_2 as a top-contact is impractical due to its poor adhesion, whereas using an adhesion layer such as chromium reduces the effective metal work-function at the contact interface. Our strategy of back-contacts circumvents this problem, since the Pt electrodes can now be deposited with an appropriate adhesion layer at the bottom without affecting the top surface work-function. The transferred WSe_2 would contact the Pt top layer, whose high work-function would still be preserved. Finally, the choice of hBN as the top-gate dielectric is motivated by its ultraflat surface, which has been shown to reduce extrinsic impurity scattering in TMDs.[21,27,28]

We evaluate the effectiveness of our back-contact scheme by performing gate-dependent transport measurements. Figure 1c shows the top-gated transfer characteristics of a WSe_2 FET with an 18 nm hBN top-gate dielectric at different values of drain bias (V_D), with the back-gate grounded. The biasing scheme is shown in Figure 1a. The top-gate bias (V_{TG}) is applied to the Pd top-gate, the back-gate bias (V_{BG}) is applied to the highly doped Si substrate, and the source terminal (V_S) is grounded. Even at a low V_D = 1 mV, the drain current (I_D) is found to increase with increasing negative V_{TG}, and an insulating behavior is observed for positive V_{TG}. This indicates predominant hole transport in the WSe_2 for negative V_{TG}, hereafter referred to as the "p-branch". For larger V_D, however, we observe an increase of I_D even with increasing positive V_{TG} (hereafter called the "n-branch"), symptomatic of emergent electron conduction in this regime. However, while I_D increases proportionally with V_D for the p-branch, the behavior is highly nonlinear for the n-branch. The overall behavior hints at the ohmic and Schottky nature of the Pt back-contacts to the valence and conduction bands of WSe_2, respectively. Similar ambipolar characteristics reported for WSe_2 FETs with conventional top-contacts[10,21,23,28] confirm that the transferred WSe_2 does indeed form a good electrical contact with the Pt electrodes. Evidence of clear subthreshold and insulating regimes along with a high I_{ON}/I_{OFF} ratio over 10^7 (at V_D = 1 V) further demonstrate that the integrity of the WSe_2 is maintained during and after transfer. The intrinsic nature of WSe_2 is evident from its insulating state around V_{TG} = 0 V, indicating no unintentional doping from the fabrication process. Negligible hysteresis in the transfer characteristics signifies minimal charge trapping and, therefore, clean interfaces in the device. A threshold voltage (V_T) of −2 V can be extracted for the p-branch from the linear region of the transfer characteristics. The quality of the hBN dielectric is manifested in the top-gate leakage current, which remains close to the noise floor throughout the measured V_{TG} range (S2 in the Supporting Information).

The nature of the contacts can be further verified from the low-bias output characteristics that are shown in Figures 1d and e. The characteristics for the p-branch (Figure 1d) show a symmetric, linear dependence of I_D on V_D for all negative values of V_{TG}, denoting ohmic contacts. On the other hand, the trend for positive V_{TG} (Figure 1e) is highly nonlinear and asymmetric, indicative of Schottky contacts to the n-branch. It should be noted that the currents for the p-branch are more than 3 orders of magnitude larger than the n-branch, confirming that Pt is better suited to contact the valence band of WSe_2. The high work-function of Pt results in a large Schottky barrier to the conduction band, which explains the Schottky nature of contacts to the n-branch. Lower work-function metals such as indium, silver,[9] and nickel,[10] would be preferable for contacting the n-branch of WSe_2. The integration of back-side source/drain contacts with a top-gated geometry ensures unimpeded electrostatic modulation of the contact and channel access regions by the top-gate. By contrast, in top-gated TMD FETs with top-contacts, screening by the source/drain electrodes obstructs modulation of these access regions by the top-gate, and the ensuing large series resistances

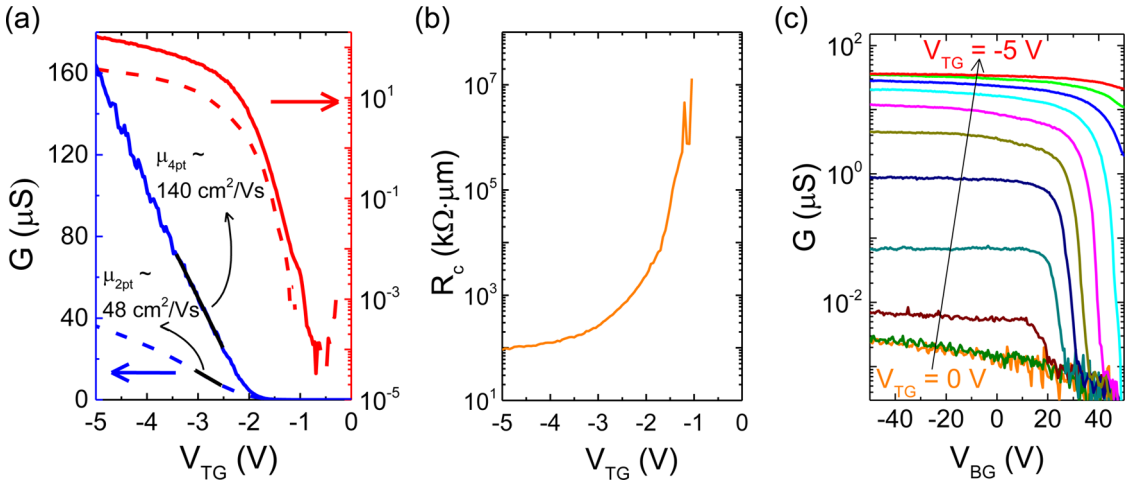

Figure 2. (a) Transfer characteristics of a WSe_2 FET (L = 6 μm, W = 12 μm) showing variation of G_{2pt} (dashed lines) and G_{4pt} (solid lines) as a function of V_{TG}, in linear (left, blue) and log (right, red) scales. The black lines show linear fits to eq 1, resulting in μ_{2pt} = 48 cm^2/(V s) and an intrinsic μ_{4pt} = 140 cm^2/(V s). (b) Plot of the variation of R_c *vs* V_{TG} shows R_c reducing with V_{TG} becoming more negative due to modulation of the channel access and contact regions by the top-gate. The back-gate is grounded in (a) and (b). (c) Back-gated transfer characteristics show saturation of G_{2pt} in the ON state, which increases as V_{TG} becomes more negative.

severely limit current injection into the channel and degrade the FET performance.[4,8] Additionally, our device structure with inert metal electrodes and dielectrics is robust, and can be extended to other TMDs and TMD heterostructures, where large series resistances are particularly problematic.[33]

In the following, we focus the discussion on hole transport in our devices. We use multiterminal four-point measurements to extract the intrinsic hole mobilities and contact resistances. Figure 2a shows the two-point conductance (G_{2pt}) and four-point, intrinsic conductance (G_{4pt}) as a function of V_{TG}. While G_{2pt} is measured as the conductance between an adjacent pair of contacts, G_{4pt} is measured using the voltage drop between the same two contacts when biasing an outer set of contacts (S3 in the Supporting Information). The field-effect mobility (μ) is then calculated using

$$\mu = \frac{1}{C_{TG}} \frac{L}{W} \frac{dG}{dV_{TG}} \quad (1)$$

where G is the channel conductance, C_{TG} is the top-gate capacitance, and W and L are the width and length of the channel, respectively. For extracting the two-point field-effect mobility (μ_{2pt}), we use $G = G_{2pt}$, and for the four-point, intrinsic field-effect mobility (μ_{4pt}), we use $G = G_{4pt}$. While G_{2pt} has contributions from both the intrinsic channel conductance and contact resistance, G_{4pt} is a measure of only the intrinsic channel conductance. The specific contact resistance (R_c) can therefore be determined using

$$R_c = \frac{L}{2}\left(\frac{1}{G_{2pt}} - \frac{1}{G_{4pt}}\right) \quad (2)$$

where R_c is normalized to the contact width and has units of kΩ·μm. For an hBN thickness of 18 nm (dielectric constant of 3.0), which corresponds to a geometric top-gate capacitance (C_{TG})[18,21] of 150 nF/cm^2, L = 6 μm, and W = 12 μm, we extract μ_{2pt} = 48 cm^2/(V s) and μ_{4pt} = 140 cm^2/(V s). The considerably lower value of μ_{2pt} compared to μ_{4pt} is due to the detrimental effect of R_c on G_{2pt}. Acting as a parasitic series resistance, R_c reduces the effective drive voltage on the channel, thereby reducing G_{2pt} and, in turn, μ_{2pt}. The extracted μ_{4pt} of 140 cm^2/(V s) compares well with prior reports of intrinsic mobilities in few-layer MoS_2[17,18,27] and WSe_2.[21,23,28] The hole density at V_{TG} = −5 V can be extracted using

$$p = \frac{C_{TG}|(V_{TG} - V_T)|}{e} \quad (3)$$

where e is the charge of an electron, to be $p = 2.8 \times 10^{12}$/cm^2. While this value is lower than the carrier densities attainable by EDL structures,[23,28] it is comparable to densities in conventional dielectric-based FETs.[21,22]

The variation of R_c *vs* V_{TG} is plotted in Figure 2b. It can be seen that R_c decreases as V_{TG} becomes more negative, asymptotically approaching ~100 kΩ·μm at V_{TG} = −5 V. While exhibiting a larger R_c than values for EDL-gated WSe_2 (~10 kΩ·μm),[21,23] our Pt contacts display superior low-temperature ohmic behavior. The strong dependence of R_c on V_{TG} is consistent with previous reports of gate-tunable contact barriers at the metal−TMD interface.[18,21,27] Variation of R_c with gate bias is not observed in traditional MOSFETs due to their highly doped source/drain regions.[34] However, if they are undoped, as in typical TMD FETs, the gate can electrostatically modulate the contact regions and, in turn, R_c. Whereas the top-gate can efficiently modulate the contact regions in our structure, screening by the source/drain electrodes prevents modulation by the back-gate. Back-gated FET transfer characteristics are

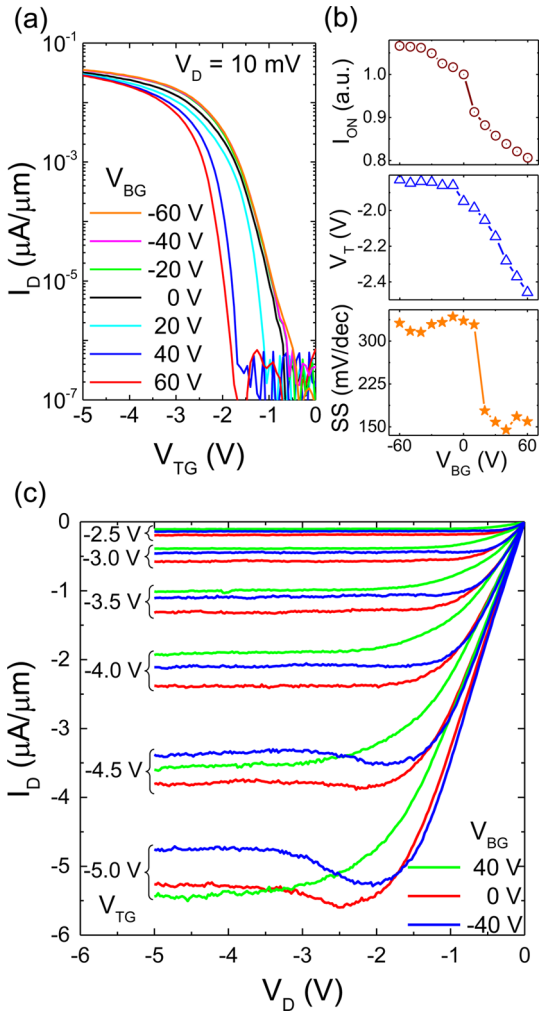

Figure 3. (a) Top-gated transfer characteristics of the FET at different values of V_{BG}. (b) The variation of I_{ON} (top panel), V_T (middle panel), and SS (bottom panel) can be understood qualitatively by considering the effect of V_{BG} on the channel. (c) FET output characteristics show current saturation and an NDR prior to the onset of saturation. The NDR magnitude changes with V_{BG}, increasing for $V_{BG} = -40$ V, and gets quenched when $V_{BG} = 40$ V.

therefore severely series resistance limited, as illustrated in Figure 2c. While the overall variation of G_{2pt} *vs* V_{BG} is consistent with hole conduction, a pronounced saturation is observed for negative V_{BG}. Similar saturation of the transfer characteristics at large gate biases has been reported in conventional top-gated FETs with top-contacts.[4,8,35] Due to our device geometry, the role played by the back-gate, which modulates the channel but not the contact regions, is analogous to the role played by the top-gate in conventional top-gated TMD FETs (S4 in the Supporting Information). Consequently, when $V_{TG} = 0$ V, the contact regions are highly resistive and inhibit current flow through the channel, resulting in a low G_{2pt} for all V_{BG}. As V_{TG} is progressively made more negative, the contact regions accumulate holes, leading to a decrease of R_c and, in turn, an increase of G_{2pt} in the ON state. The G_{2pt} saturation is due to R_c dominating the total channel resistance. Since R_c can be modulated much more effectively by V_{TG}, G_{2pt} in the ON state is highly sensitive to V_{TG} as compared to V_{BG}. Further, the shift in V_{BG} at the onset of saturation with varying V_{TG} is due to the effect of dual gating of the channel. A more negative V_{TG} accumulates additional holes in the channel, thereby requiring a more positive V_{BG} to deplete them. The effect is an increase of V_{BG} at the onset of saturation as V_{TG} is made more negative. Finally at $V_{TG} = -5$ V, the FET remains ON throughout the measured V_{BG} range. The intrinsic nature of WSe_2 is therefore the primary reason why top-gated FETs in the conventional top-contact geometry show poor characteristics.[8,21] On the other hand, our structure with back-contacts is better suited for top-gated operation since it allows for efficient top-gate modulation of the contact regions.

The back-gate can further be used to tune the FET characteristics. Figure 3a shows the top-gated transfer characteristics at different V_{BG} values. Variation in FET parameters such as ON current (I_{ON}), V_T, and subthreshold swing (SS) are apparent and are shown in Figure 3b. A negative (positive) V_{BG} increases (reduces) the hole density in the channel, leading to a V_T shift. As a consequence, negative (positive) values of V_{BG} reduce (increase) the channel resistance and increase (reduce) I_{ON}. At negative values of V_{BG}, which increase the channel hole density, the FET turn-ON is limited by the contact regions' turn-ON. The relative insensitivity of the contacts to V_{BG} makes V_T insensitive to V_{BG} in this regime. Two predominant regimes are evident in the SS, at ~330 mV/dec for $V_{BG} \leq 10$ V and ~150 mV/dec for $V_{BG} > 10$ V. For $V_{BG} \leq 10$ V, the channel accumulates excess holes, and the SS is determined by turn-ON of the contact regions. In contrast, for $V_{BG} > 10$ V, the channel is populated with electrons, resulting in a steeper SS of 150 mV/dec, dictated by diffusion current from the source to drain.[34] It is to be noted that the SS is relatively insensitive to the carrier concentration in the channel, but depends only on the polarity of excess carriers induced by the back-gate.

Figure 3c shows the top-gated FET output characteristics at different values of V_{BG}. First, there is clear evidence of current saturation at large negative V_D for all values of $V_{TG} < V_T$ and V_{BG}. Current saturation is due to channel pinch-off at the drain, similar to a conventional MOSFET. A maximum drive current of ~5 μA/μm is obtained at $V_{TG} = -5$ V for a long-channel device with $L = 6$ μm, which is comparable to values reported for WSe_2 p-FETs with chemically doped source/drain contacts.[8] Higher drive currents are possible by using shorter channel lengths and thinner top-gate dielectrics. A second feature is the negative differential resistance (NDR) behavior prior to the onset of current saturation. The NDR behavior that is commonly observed in bulk III–V FETs is due to a transferred electron mechanism, often referred to as the Gunn effect.[34]

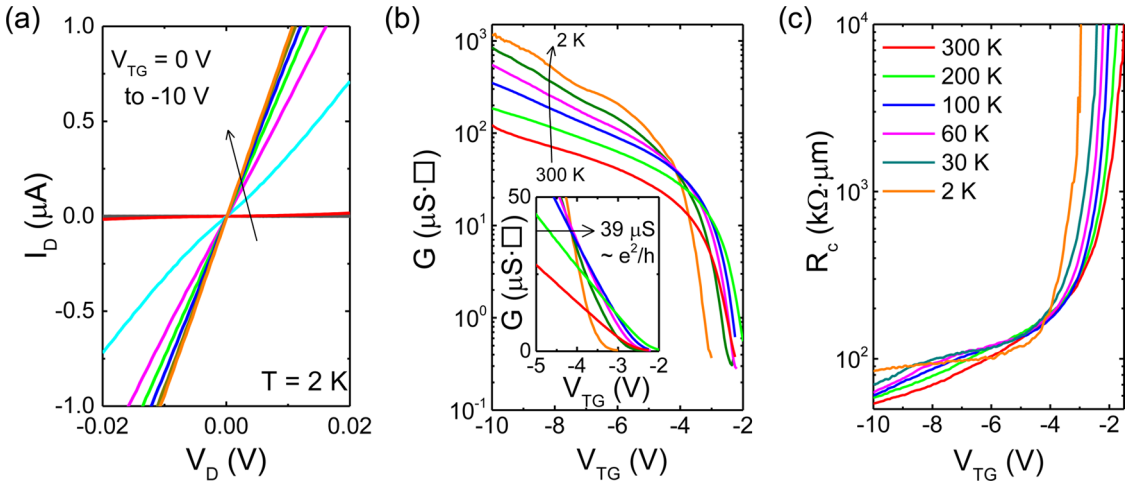

Figure 4. (a) Low-bias output characteristics showing a mostly linear I_D-V_D behavior, indicating the ohmic nature of the Pt back-contacts even at 2 K. (b) Variation of G *vs* V_{TG} with temperature shows G increasing with reducing temperature for $V_{TG} < -4$ V, characteristic of a metallic phase. The inset shows a close-up of the crossover, at $G_c = 39\ \mu S$ ($\sim e^2/h$). (c) Variation of R_c roughly mirrors G, but with a weaker temperature dependence at large negative V_{TG}. The back-gate is grounded for all measurements.

Recent reports of NDR in MoS_2 have also been attributed to a transferred electron mechanism between satellite valleys and/or a self-heating effect.[36,37] Our devices, however, also show considerable hysteresis between the forward and reverse I_D-V_D sweeps (S5 in the Supporting Information). Both the NDR amplitude and hysteresis are correlated, increasing for $V_{BG} = -40$ V and almost vanishing for $V_{BG} = 40$ V. The NDR dependence on the V_{BG} value and polarity suggests that the vertical carrier distribution in the WSe_2 layer plays a key role. Application of V_{BG} changes the position of the charge centroid in the WSe_2, with negative (positive) V_{BG} shifting the holes closer to (further away from) the SiO_2 substrate. A real space transfer between the high-mobility top layer closer to the hBN and the low-mobility bottom layer closer to the SiO_2 substrate could lead to an NDR behavior. The hysteresis dependence on V_{BG} is further suggestive of hot carrier trapping at the WSe_2-SiO_2 interface,[29] which increases (decreases) when the carriers are closer to (further away from) the SiO_2 substrate. It is also possible that a transferred electron mechanism could be at play, as evinced by the persistent NDR in both the forward and reverse sweeps, but the hysteresis makes it difficult to unambiguously draw this conclusion.

We now proceed to discuss the temperature dependence of transport in our devices. The ohmic nature of the Pt back-contacts is retained down to 2 K, as shown in Figure 4a. While the I_D-V_D for small V_{TG} shows a slight nonlinearity, the behavior is more linear for large negative V_{TG}, where the channel has a large concentration of holes. This enables use of a standard low-frequency lock-in technique (10 nA excitation at 11.27 Hz) to measure the channel conductivity, $G = G_{4pt} \times (L/W)$, as a function of temperature (Figure 4b). Two distinct regimes are apparent in the temperature variation of G; for $V_{TG} < -4$ V, G increases monotonically with decreasing temperature, and for $V_{TG} > -4$ V, G does not follow a monotonic trend. The crossover between these two regimes, apparent from Figure 4b and Supporting Information S6, suggests a metal−insulator transition (MIT), consistent with previous observations for a variety of 2D electron and hole systems, including TMDs.[17,18,23,28] A close-up of the MIT point in the inset of Figure 4b shows the crossover at a conductivity $G_c = 39\ \mu S \approx e^2/h$. Other samples show G_c in the same range of conductivity, albeit with slight variations (S6 in the Supporting Information). To better understand the nature of the MIT observed in our samples, we discuss the results using the theoretical framework developed to explain the phenomenon in a large set of 2D electron and hole systems.[38,39]

According to the scaling theory of localization, all noninteracting 2D systems exhibit an insulating ground state in the limit of zero temperature.[40] At high carrier densities and in samples with reduced disorder, the localization length can exceed the sample size. In this weakly localized state, the 2D system can exhibit an apparent metallic behavior, explained in terms of the temperature-dependent screening of fixed charged impurities. For high sample disorder or at low carrier densities, the system becomes strongly localized, and the temperature dependence of conductivity displays the expected insulating behavior. This crossover from a metallic weakly localized regime at high carrier densities to an insulating strongly localized regime at low carrier densities has been used to explain the MIT in 2D semiconductors.[17,38] To ascertain the nature of the MIT in our devices, we examine the following temperature scales: the Fermi temperature (T_F), the Bloch−Grüneisen temperature (T_{BG}), and the Dingle temperature (T_D) (S7 in the Supporting Information). The temperatures T_{BG} and T_D define scales associated with

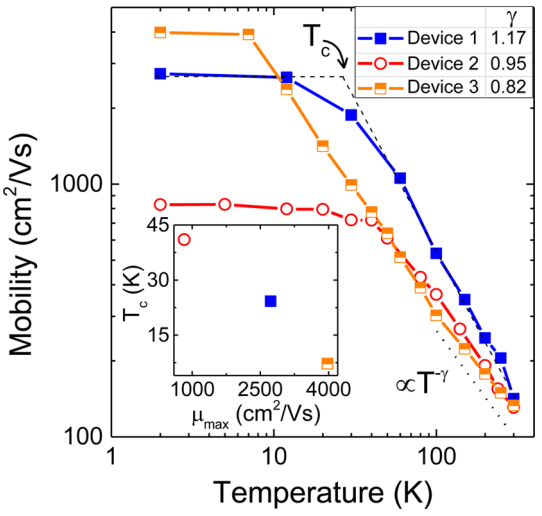

Figure 5. Temperature dependence of μ_{4pt} for three different WSe_2 devices. For $T > 100$ K, μ_{4pt} follows a power law trend, $\propto T^{-\gamma}$, with the γ values for the three devices shown in the inset table. At low temperatures, μ_{4pt} saturates to $\mu_{max} \approx$ 4000 $cm^2/(V\,s)$, limited by Coulomb scattering and/or defects in the WSe_2. The inset shows variation of T_c with μ_{max}.

phonon scattering and disorder, respectively. An unambiguous manifestation of a weak localization-mediated metallic phase requires $T_D < T_F < T_{BG}$ at the crossover point, a condition that rules out phonon scattering in the metallic phase and ensures that the disorder is sufficiently weak.[38] For the sample of Figure 4, μ_{4pt} = 2600 $cm^2/(V\,s)$, and with the crossover carrier density (p_c) of 5.3 × $10^{11}/cm^2$ at 2 K, we obtain $T_F = 29$ K, $T_{BG} = 16$ K, and T_D = 5.0 K. Since $T_F > T_{BG}$, the temperature dependence of G in the metallic phase can potentially be affected by phonon scattering in our devices. We note that in the absence of a more reliable carrier density measurement, *e.g.* through Hall effect, and the uncertainty in V_T, the value of p_c could be underestimated. However, a larger p_c will only increase T_F and T_{BG}, but still maintain the relation $T_F > T_{BG}$. For acoustic phonon scattering at $T > T_{BG}$, G is expected to follow a $\sim T^{-1}$ law, resulting in an apparent metallic behavior.[41] The metallic phase in our devices does not stem solely from a quantum electronic mechanism.

The insulating phase, on the other hand, for $p < p_c$, is the expected behavior for a 2D system. While a strong localization effect at low carrier densities results in an insulating behavior, an alternate semiclassical percolation model can also explain this phenomenon.[20,39] Density inhomogeneities induced by disorder are believed to block conductive paths in the channel at low carrier densities, leading to an insulating state due to percolation of carriers between the potential fluctuations. The similar values of $G_c = O(e^2/h)$ expected for both the localization and percolation mechanisms make it difficult to choose one to explain the insulating phase in our devices, as is the case for other 2D systems.[38] The variation of R_c *vs* V_{TG} as a function of temperature is shown in Figure 4c. The variation of R_c roughly resembles G, with R_c increasing on reducing the temperature for $V_{TG} > -4$ V and varying weakly for large negative V_{TG}. The weak temperature dependence of R_c when the channel is populated with holes ($V_{TG} < -4$ V) is consistent with prior reports of contact behavior in MoS_2 FETs.[18,27]

Finally, to determine the scattering mechanisms limiting hole transport in WSe_2, the variation of μ_{4pt} with temperature in the metallic regime is shown for three different three/four-layer WSe_2 FETs in Figure 5. All three devices show a modest μ_{4pt} of around 140 $cm^2/(V\,s)$ at room temperature, which then increases rapidly with decreasing temperature. The variation in the high-temperature regime ($T > 100$ K) follows a power law dependence, $\mu_{4pt} \propto T^{-\gamma}$, with varying values of γ (from ~ 0.8 to 1.2) for the three samples measured. Acoustic phonon scattering is expected to result in $\gamma = 1$, whereas $\gamma > 1$ is a signature of optical phonon scattering being the dominant scattering mechanism.[41] The values of γ closer to 1 in our devices suggest that acoustic phonon scattering is the mobility-limiting factor.[42] Lowering of γ below 1 has been attributed to homopolar phonon quenching by the top-gate dielectric and/or the collective effect of multiple scattering mechanisms.[17,43] At low temperatures, μ_{4pt} saturates to an upper limit (μ_{max}), likely limited by Coulomb scattering or defects.[41,44] A critical temperature (T_c) can be defined at the crossover of the two regimes of temperature dependence of μ_{4pt}. There is a considerable variability in μ_{max} between samples ($\mu_{max} \approx$ 800 $cm^2/(V\,s)$ to 4000 $cm^2/(V\,s)$), which varies inversely with T_c (~ 40 to 7 K), as shown in the inset of Figure 5. The value of T_c can be an indicator of sample quality, with cleaner samples transitioning to a Coulomb scattering dominated transport regime at lower temperatures.[44] We also note that μ_{max} does not seem to depend on γ. We attribute the high values of μ_{max} in our devices to the cleaner top hBN–WSe_2 interface, where the holes reside at negative V_{TG} values. The hole mobilities in our devices compare very well with recent reports of electron mobilities in hBN-encapsulated WSe_2,[45] underlining the high material quality of WSe_2.

CONCLUSION

To summarize, we successfully used high work-function Pt electrodes to contact the valence band of WSe_2. Our structure with back-contacts and an hBN top-gate dielectric provides a device design for optimized top-gated operation, resulting in stable ohmic p-type contacts without the need for any additional doping of the channel access regions. We observed saturating output characteristics, with a signature of a back-gate-tunable negative differential resistance. The ohmic Pt contacts down to cryogenic temperatures enabled us to perform temperature-dependent transport measurements, which revealed a metal–insulator transition. The temperature dependence of mobility indicated a phonon-dominated scattering mechanism at high

temperatures, with a crossover to Coulomb scattering at low temperatures. Our findings highlight the significance of Pt as a p-type contact for WSe_2 in order to study its intrinsic electrical properties. Moreover, the combination of our back-contact geometry and an hBN top-gate dielectric provides a viable platform to explore the transport properties of other 2D materials and their heterostructures.

MATERIALS AND METHODS

Device Fabrication. The FETs are fabricated using commercially available sources of WSe_2 crystals (HQ Graphene and nanoScience Instruments). Both source materials result in devices with very similar characteristics. Individual flakes of WSe_2 and hBN are exfoliated onto 300 nm SiO_2/Si substrates, and three/four-layer WSe_2 and 15−20 nm hBN flakes are identified using optical contrast, Raman, and photoluminescence measurements. On a separate substrate, thin Cr/Pt (2 nm/8 nm) electrodes are patterned using a combination of e-beam lithography (EBL), e-beam metal evaporation (EBME), and lift-off. Using a silicone stamp spin-coated with a heat-release polymer,[30] we first "pick up" the hBN flake. A custom-built micromanipulator−microscope setup is then used to align and "pick up" the WSe_2 using the hBN, resulting in an hBN/WSe_2 stack supported on the polymer. This stack is then aligned and stamped onto the prepatterned Cr/Pt electrodes, after which the polymer is washed away in acetone. This leaves the hBN/WSe_2 stack on the Cr/Pt electrodes. A 3 h 200 °C forming gas (1 Torr) anneal is performed to clean any remaining polymer residues. A local Pd top-gate (30 nm) is then patterned using EBL, EBME, and lift-off. Finally, thick Cr/Au (10 nm/80 nm) contact pads are patterned for electrical probing.

Electrical Characterization. Room-temperature electrical measurements are done in ambient conditions, on a Cascade Summit probe station using an Agilent B1500A dc parameter analyzer. Temperature-dependent measurements are done in a PPMS EverCool II Helium refrigerator. An Agilent B1500A is used for dc measurements, and an SR830 lock-in amplifier is used for the low-frequency lock-in measurements.

Conflict of Interest: The authors declare no competing financial interest.

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S1: Raman and photoluminescence characteristics, S2: Transfer characteristics and top-gate leakage, S3: 2-point and 4-point measurement scheme, S4: Top contacts *vs* back contacts, S5: Hysteresis in output characteristics, S6: Metal−insulator transition, S7: Temperature scales for MIT (PDF)

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